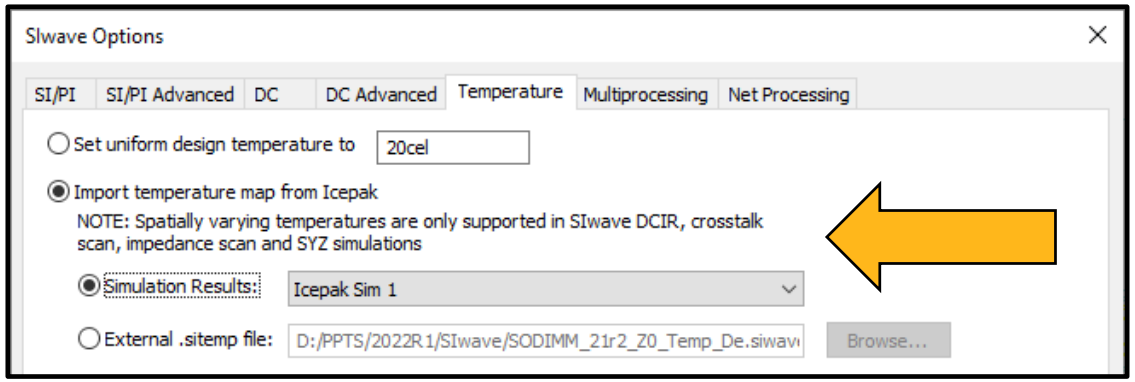
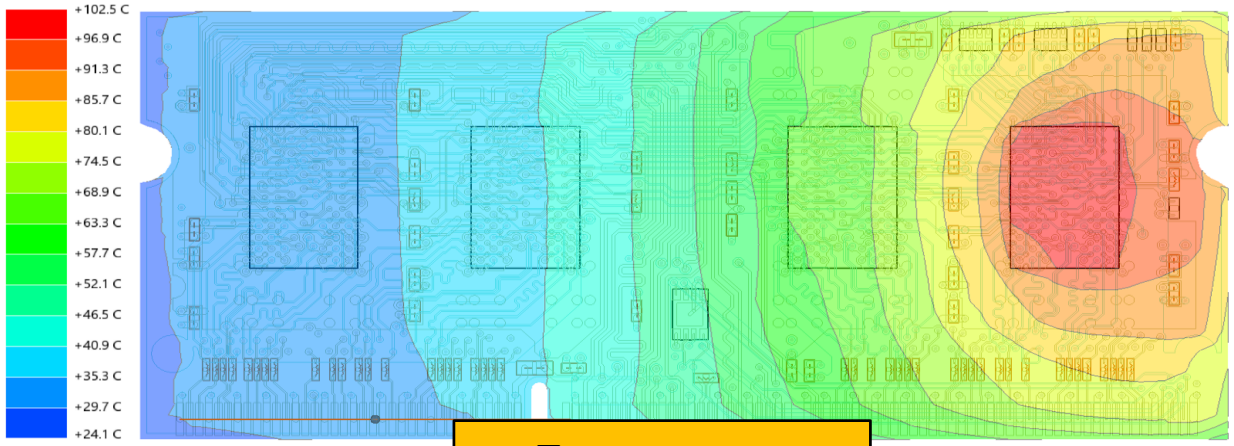
Ansys 2022 R1
Siwave新功能介绍

新科益系统与咨询（上海）有限公司

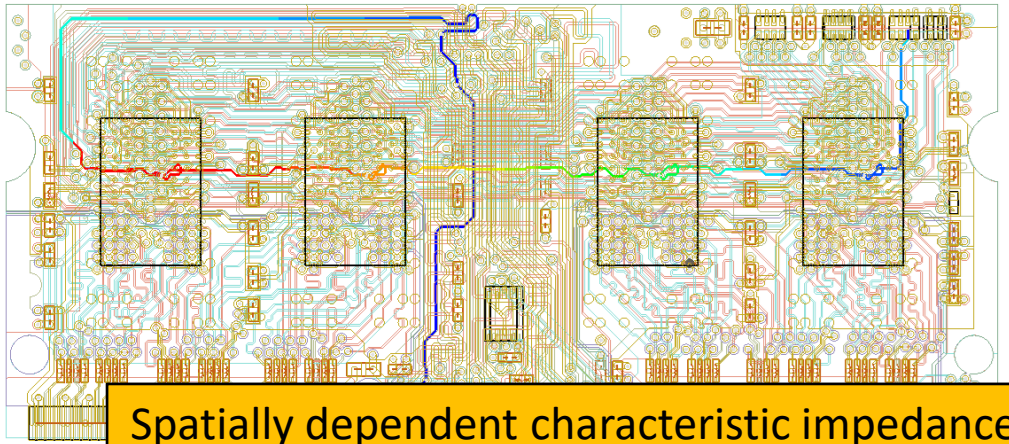
Temperature dependent materials in SIwave AC

- Temperature map import from Icepak
- Thermal modifier applied to dielectric materials and conductors
- Non-uniform temperature distribution supported
- Spatially dependent permittivity and conductivity for plane (FEM) and trace (MoM) models



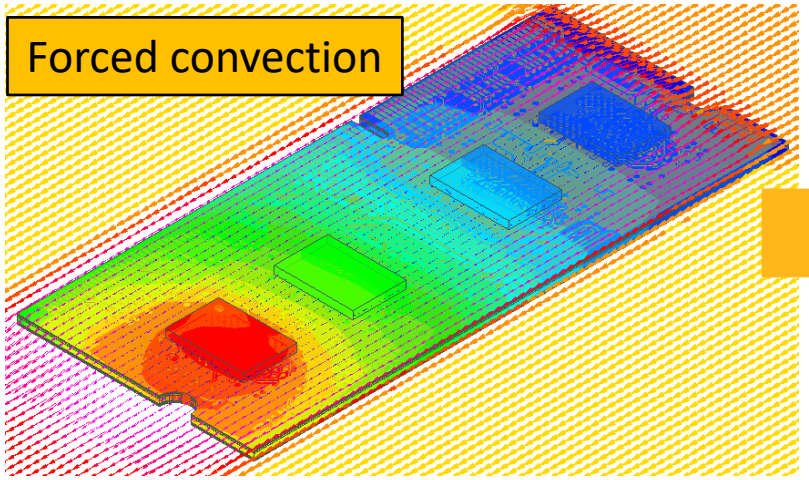


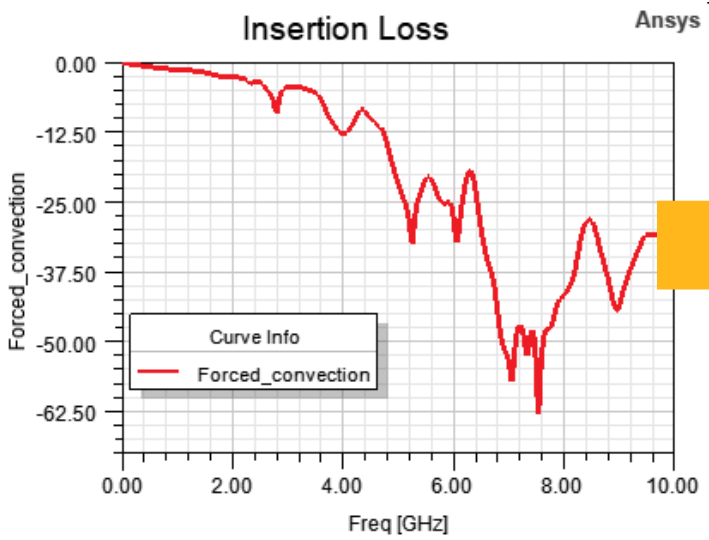
Temperature

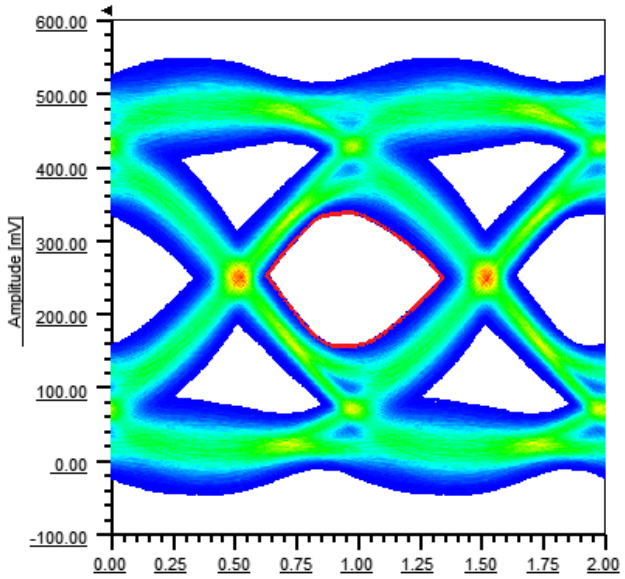


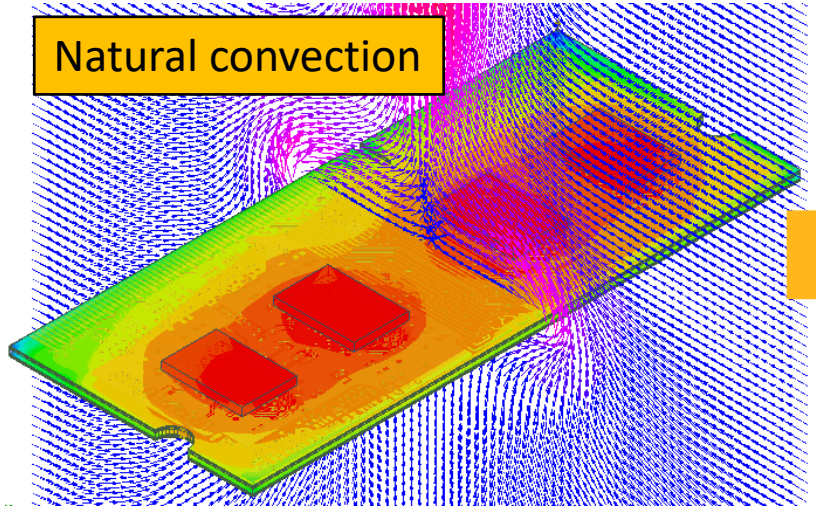
Spatially dependent characteristic impedance

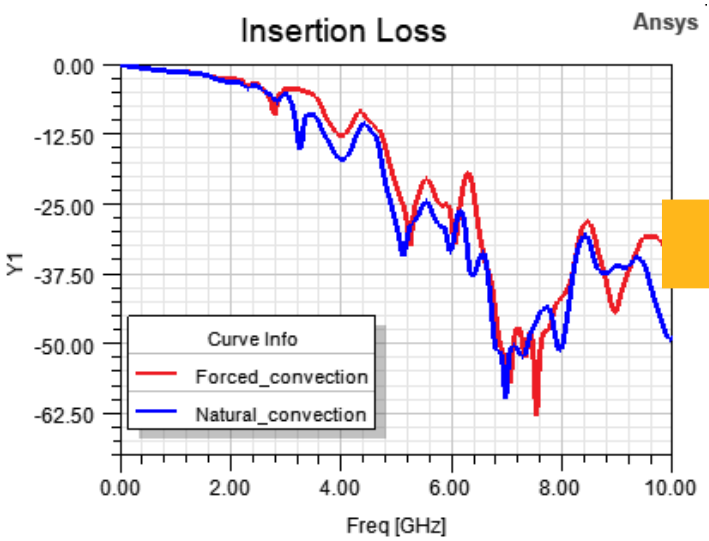
Temperature dependent materials in SIwave AC

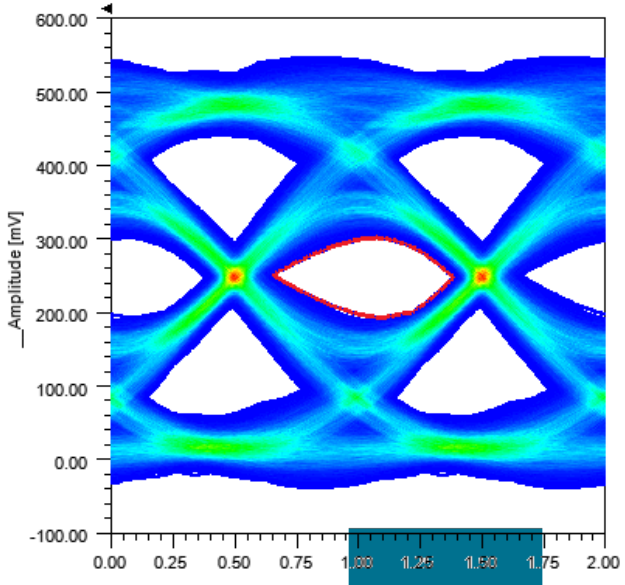








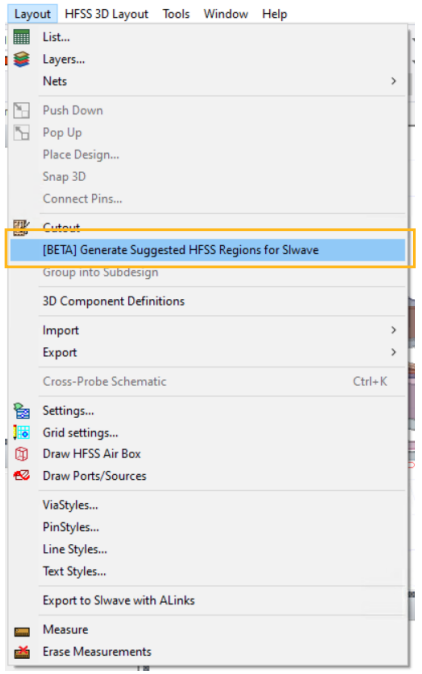




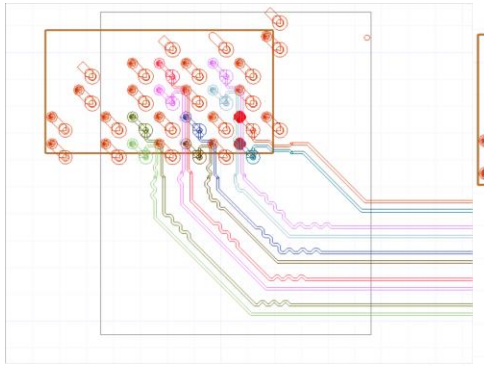
SIwave HFSS Regions

[BETA] Auto (suggested) SIwave HFSS Regions in 3D Layout

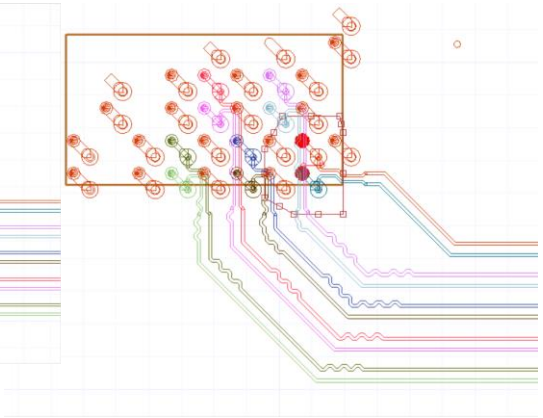
- Creates HFSS Regions around areas of significant 3D activity
- Guarantees Electrical Coherence for HFSS Simulations
- Regions are a suggestion; users can modify or remove regions they dislike



User-Defined HFSS Region

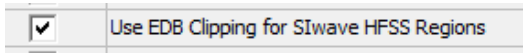


Auto HFSS Region

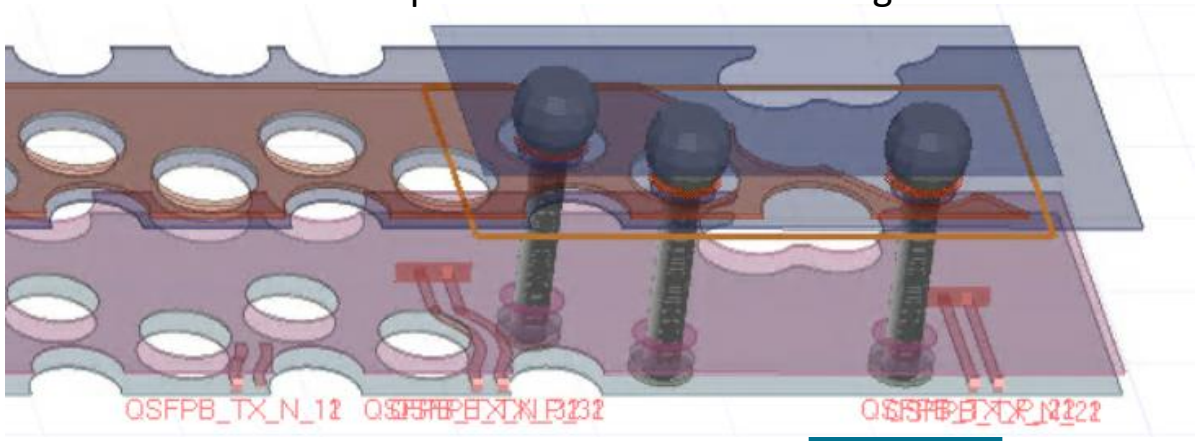


[BETA] EDB-based Region Clipping

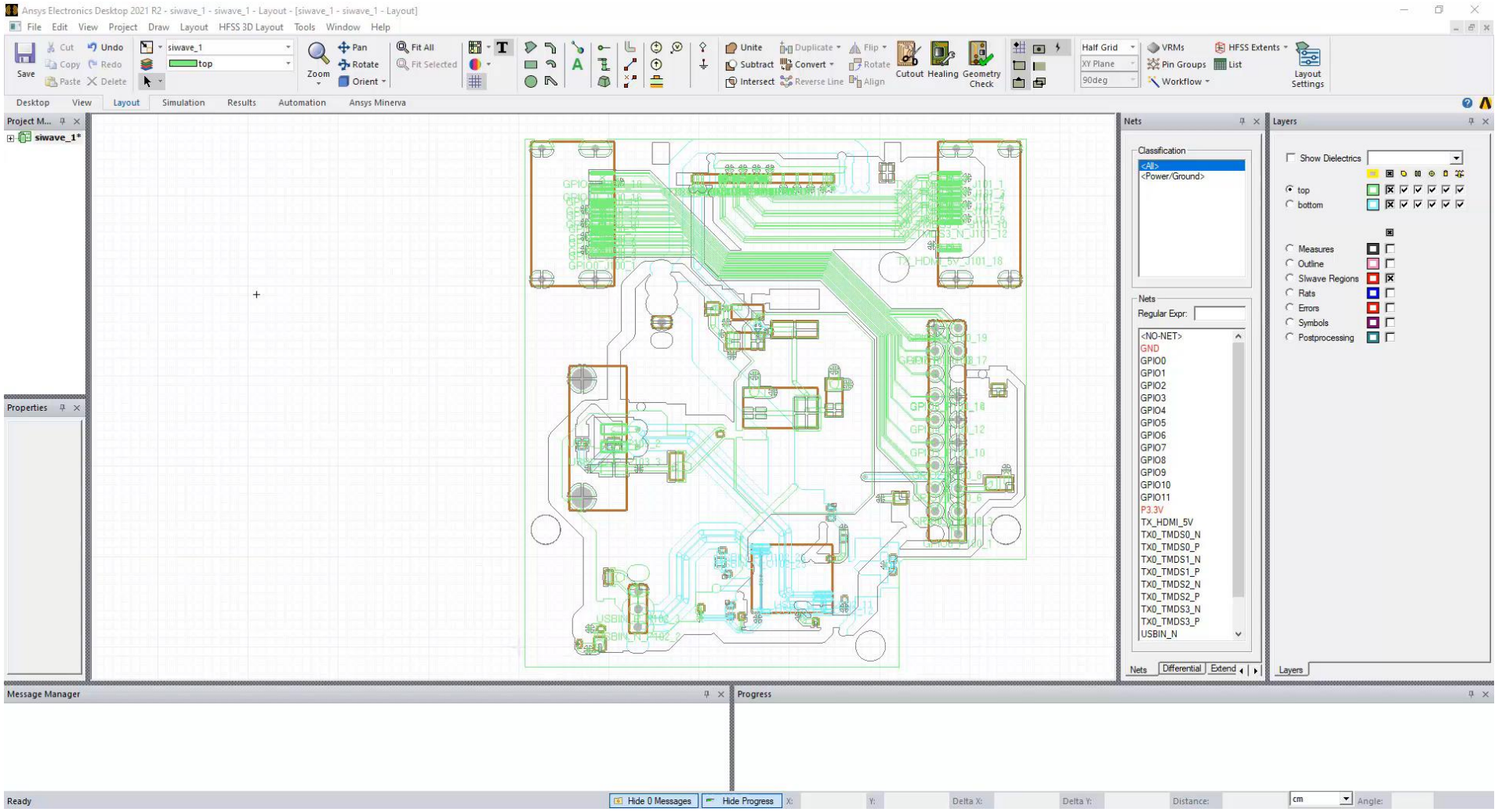
- When launched from 3D Layout, replaces ClipDesign during preparation HFSS Regions
- Operates directly on an EDB, preserving EDB-only elements such as waveports
- Activate through Beta Feature



Waveports in an SIwave HFSS Region

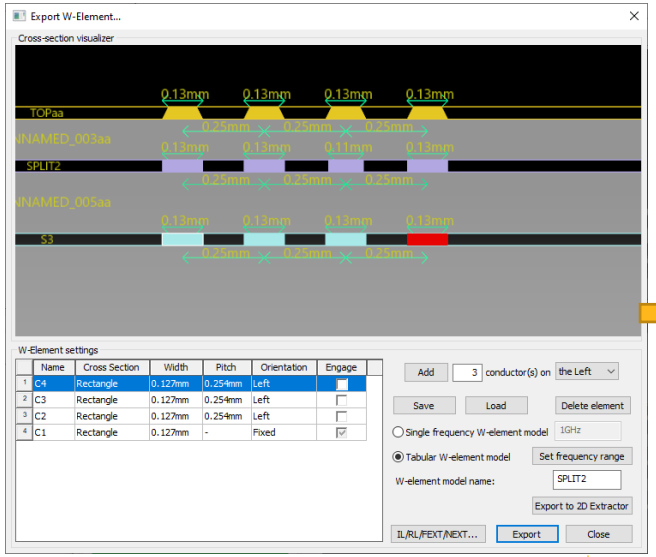


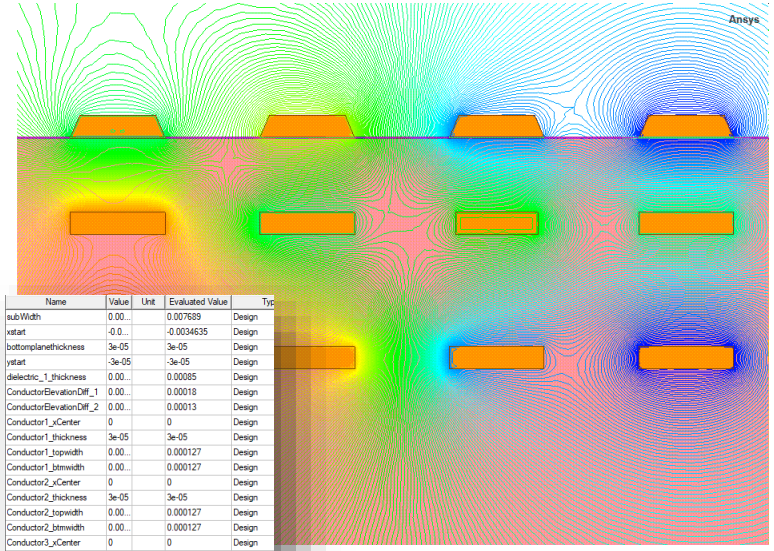
SIwave HFSS Regions

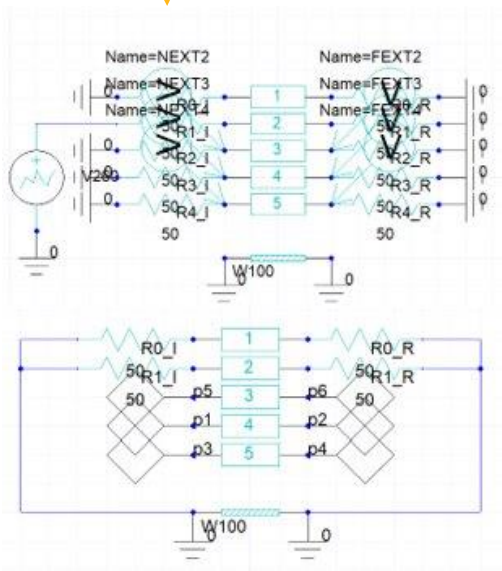


Stackup Wizard

- Ability to define/engage multiple conductors in one simulation
  - Multiple ports for linear network analysis
  - Multiple victims for cross talk analysis
- Engage multiple conductors across selected layers
- Fully parameterized 2D extractor export
  - Conductor pitch/width/thickness/etch
  - Conformal, dielectric, signal layer thickness and elevation
- Circuit schematic and Touchstone file export supports multi-layer conductor models
- Supported in W-element cross section analysis feature in SIwave and 3D layout
- Available in SIwave, 3D Layout, SIXplorer








```
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+ GMODEL=g_METAL_2 CMODEL=c_METAL_2

.model r_METAL_2 sp N=5 SPACING=nonuniform VALTYPE=real INTERPOLATION=spline
+ DATA = 201
+ 0
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+         0.1762478313507305
+          4.055073096384399
+           0.1762480162309 2
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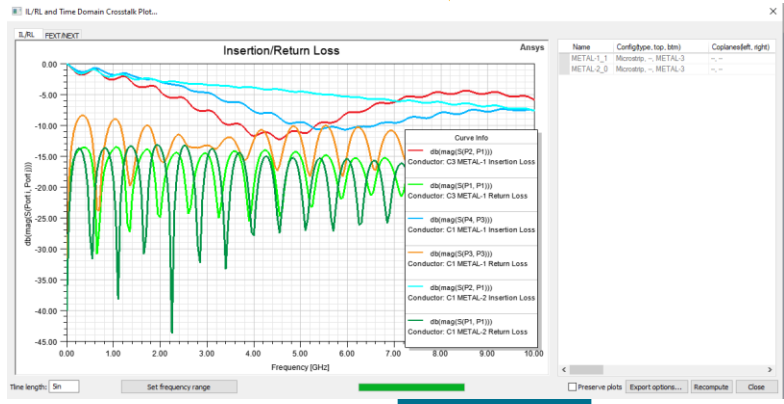


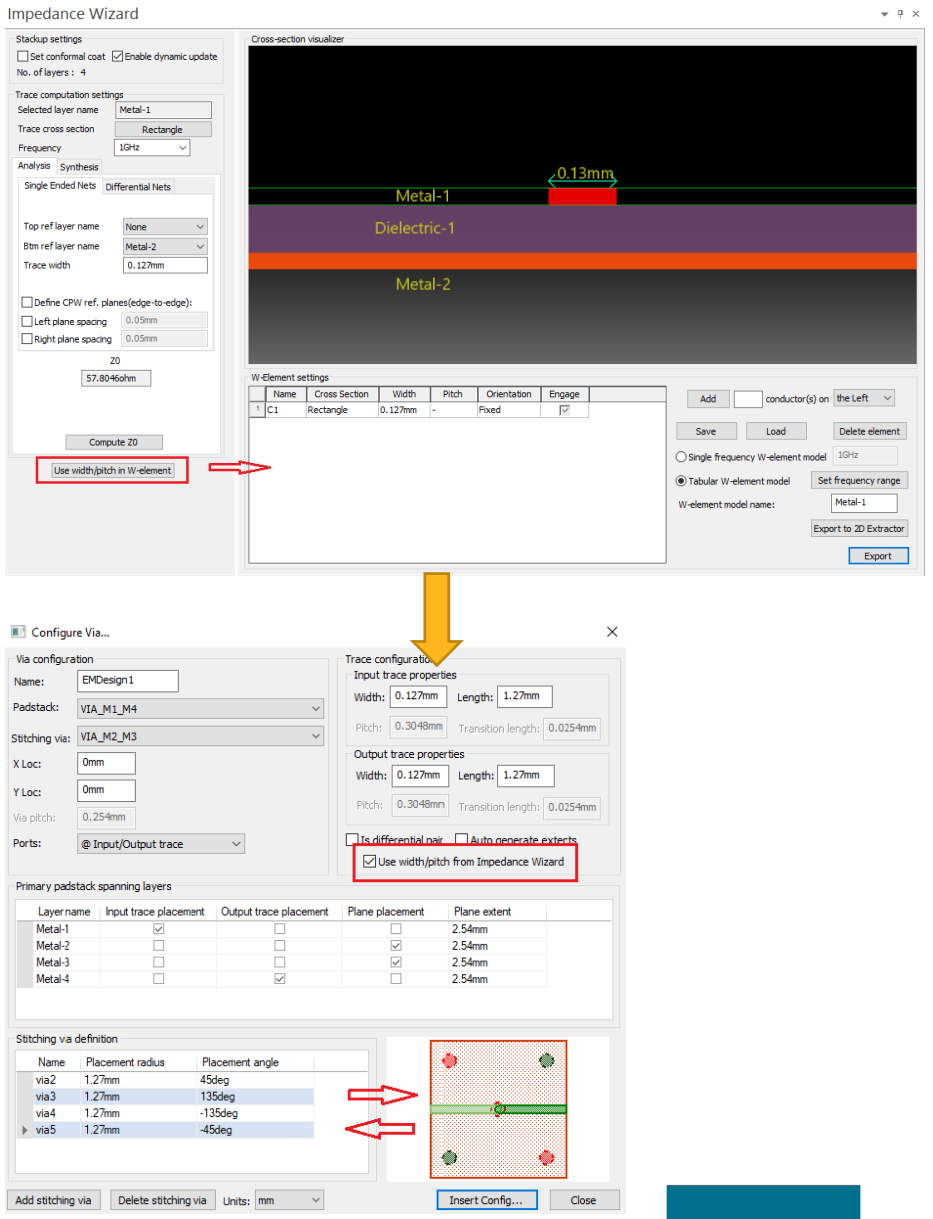
SIXplorer

Via Wizard

- Freeform stitching via placement
  - Stitching via location is defined using placement radius and angle
  - Support copy/paste of entire grid row to add new definition
  - Allow bulk updates to values of placement radius and angle by clicking on corresponding column header
- Addition of 2D top-down EDB preview in via configuration dialog
  - Two-way selection between grid row and 2D view
- Propagate synthesized/analyzed trace width/pitch from Impedance wizard to Via wizard
- Allow import of stackup and padstacks from unsourced/non-SIXplorer AEDT projects/EDBs

Impedance Wizard

- Ability to save/restore UI state at application close/launch



EMI Scanner

- Rule-checking Improvements
  - Use more appropriate distance metrics in various rules
  - Proper handling of curved traces
- Edge-to-edge vs center-to-center
- Distribution of vias over grid rather than just simple count
- Additional details and images in exported reports

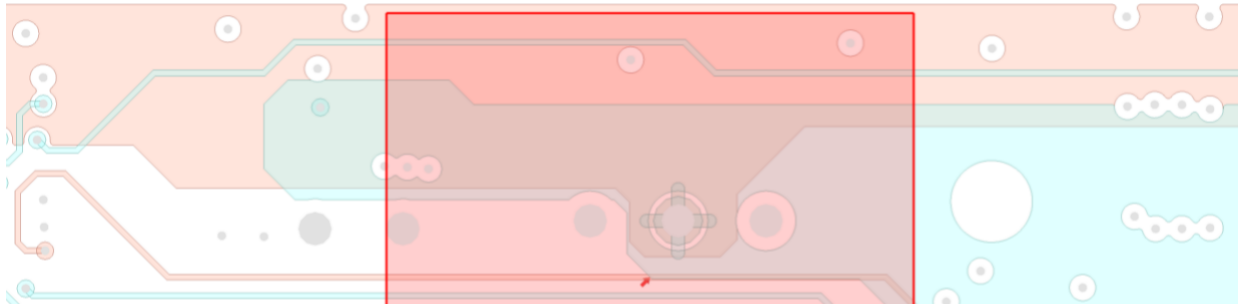
EMI Violations

Rule Type: Signal Reference

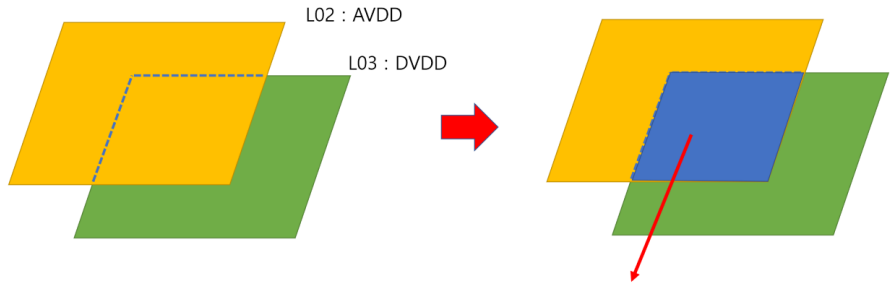
Rule Name: Critical Net Crossing Split Reference Plane

Rule Description: Critical nets must not cross a split in the adjacent reference plane. Notes: 1. Any crossing of an adjacent plane by a critical net will cause a violation. 2. A crossing is allowed if two stitching capacitors (one on either side of the crossing point) are within a specified distance of the crossing.

Violation 1: Cap Search Box = [(23.622, 51.1302) (38.862, 66.3702)], Gap Point = (31.242, 58.7502), Net = A0_GPIO, Reference Layer = LYR_1, Signal Layer = LYR_2



- New Rule: Disparate Reference Overlap
  - Requested for CMOS image sensor development
- Power supply noise sensitive to coupling of digital reference and analog reference
  - Define a set of nets whose planes cannot overlap with planes from the other set
  - Violations issued if total overlap area exceeds a threshold



Disparate Reference Overlap

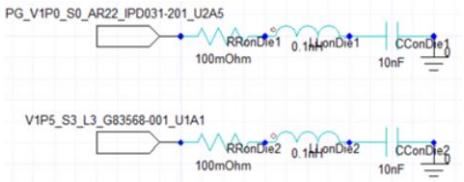
This rule checks for overlapping reference planes from different domains.

Rule State	(•) On ( ) Off
Maximum Total Overlap Area	0.64516 mm2
Nets to Include in Reference Group A	All Nets; Power Nets; Ground Nets; All Critical Nets Only; All Single-Ended Critical Nets Only; I/O Nets Only; Exclude Power Nets
Nets to Include in Reference Group B	All Nets; Power Nets; Ground Nets; All Critical Nets Only; All Single-Ended Critical Nets Only; I/O Nets Only; Exclude Power Nets
Sort by Column	Index
Log File State	( ) On (•) Off
Weighting Factor	0.6

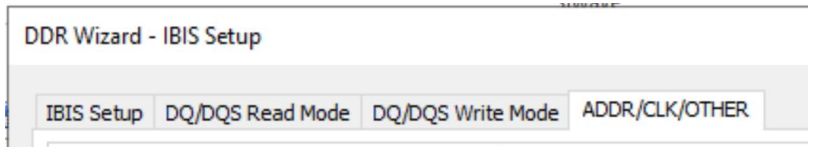
CAD-IT CONSULTANTS

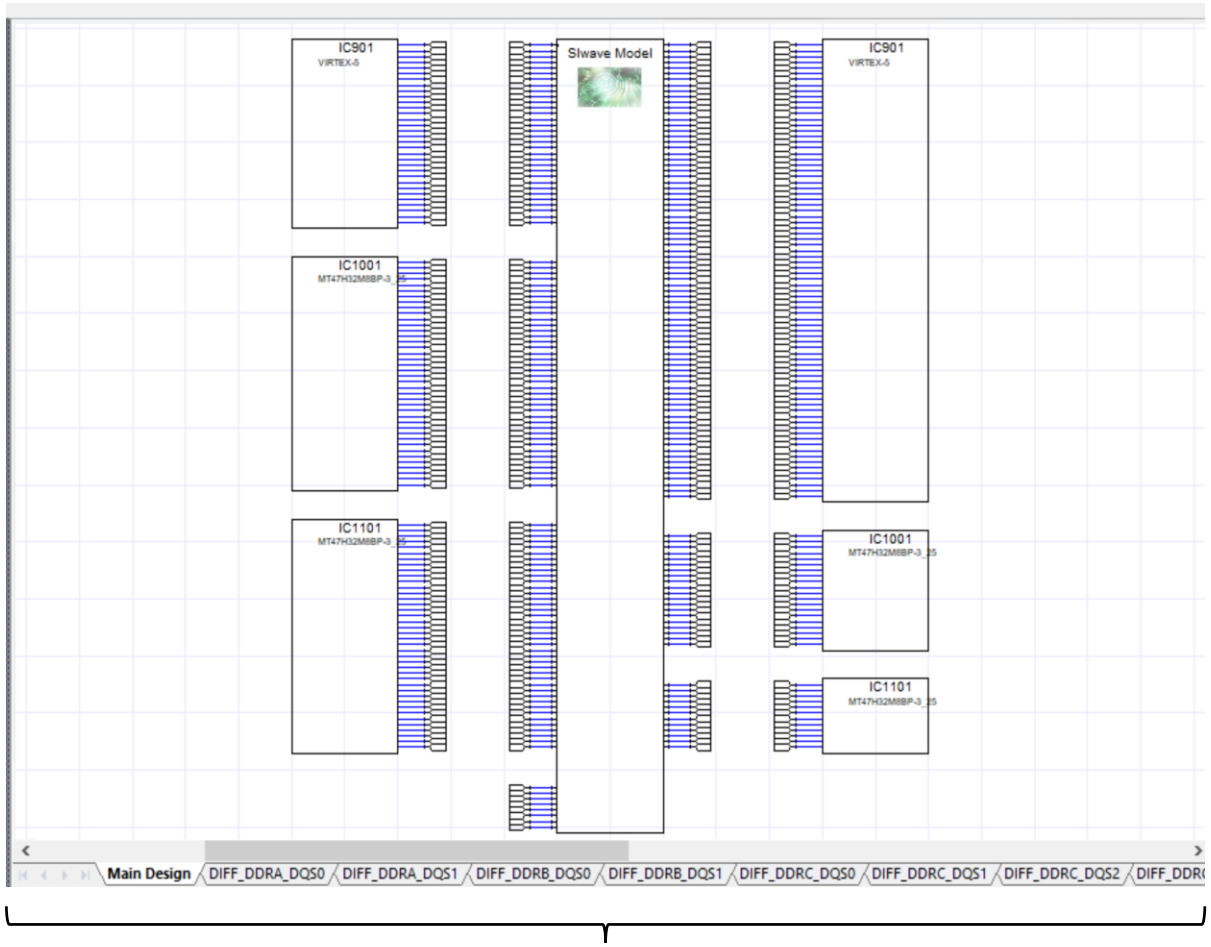
DDRwizard

- Schematic organized in multiple tabs
- Main tab contains dynamic-link block along with driver/receiver components
- Nets grouped by byte lanes with corresponding strobe
- Separate tab for IBIS blocks
- OnDie RLC support for VRM nets



- New tab for ADDR/CLK/OTHER nets in IBIS assignment dialog



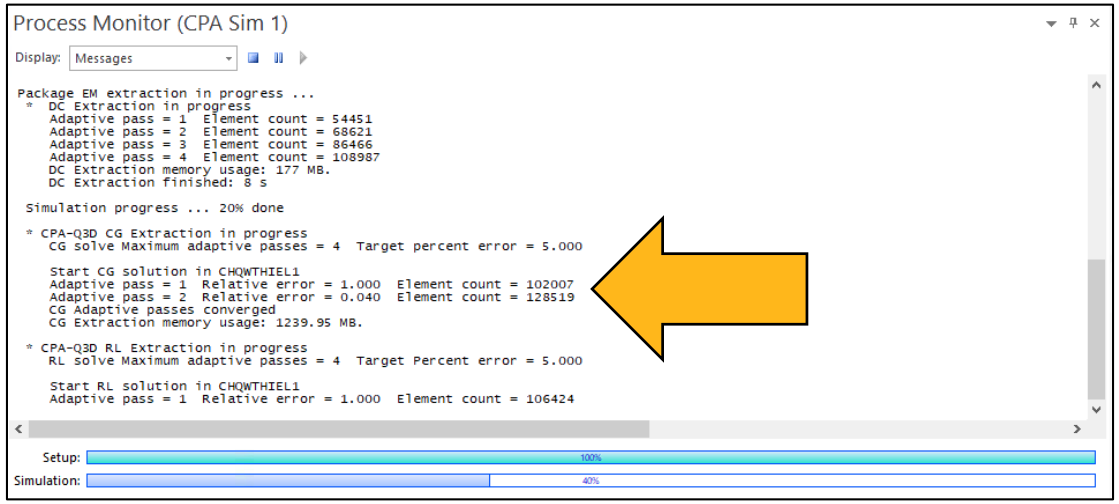


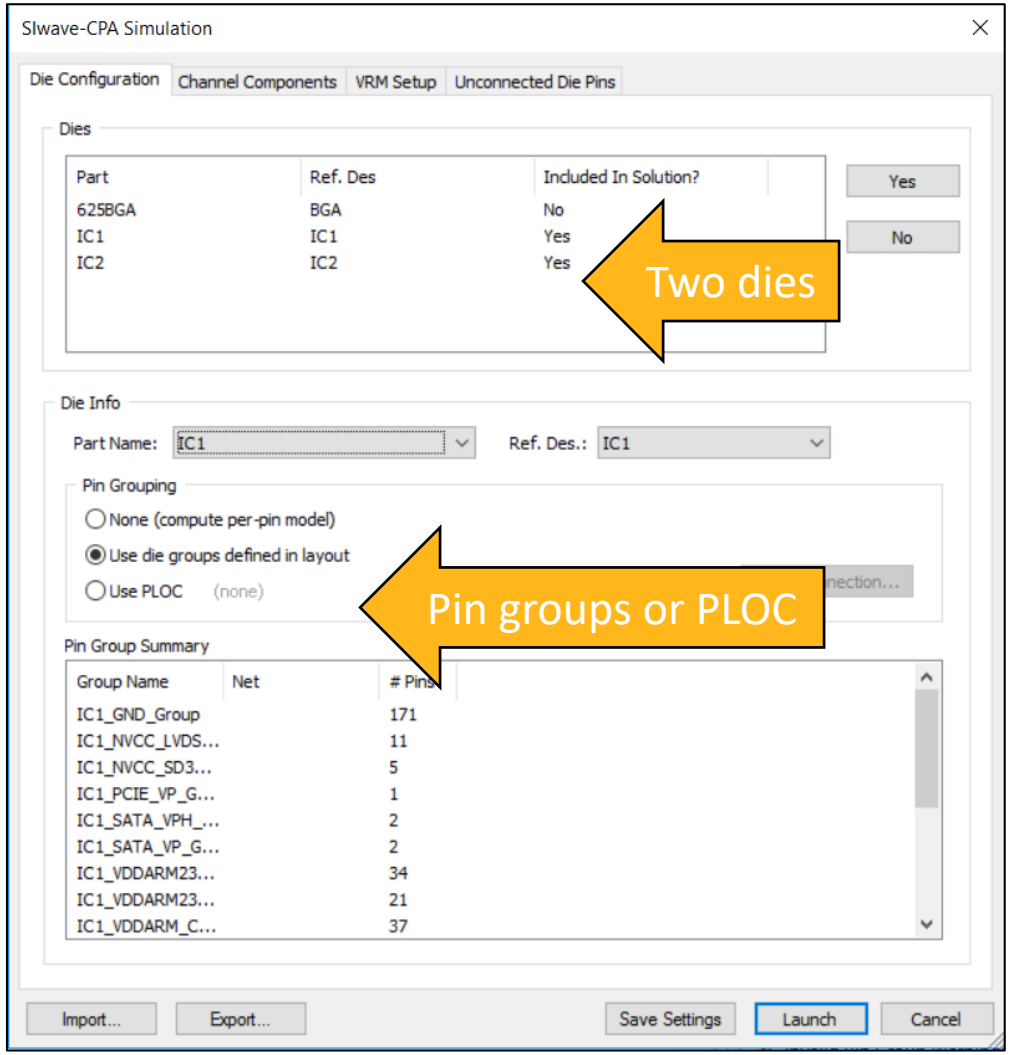
DDR schematic organized into logical tabs

CPA Solver

- Multi-Die and Multi-PLOC support
  - Extract RLCG for multiple dies
  - Import and connect PLOC/CPM or set the Pin Grouping model for each die individually

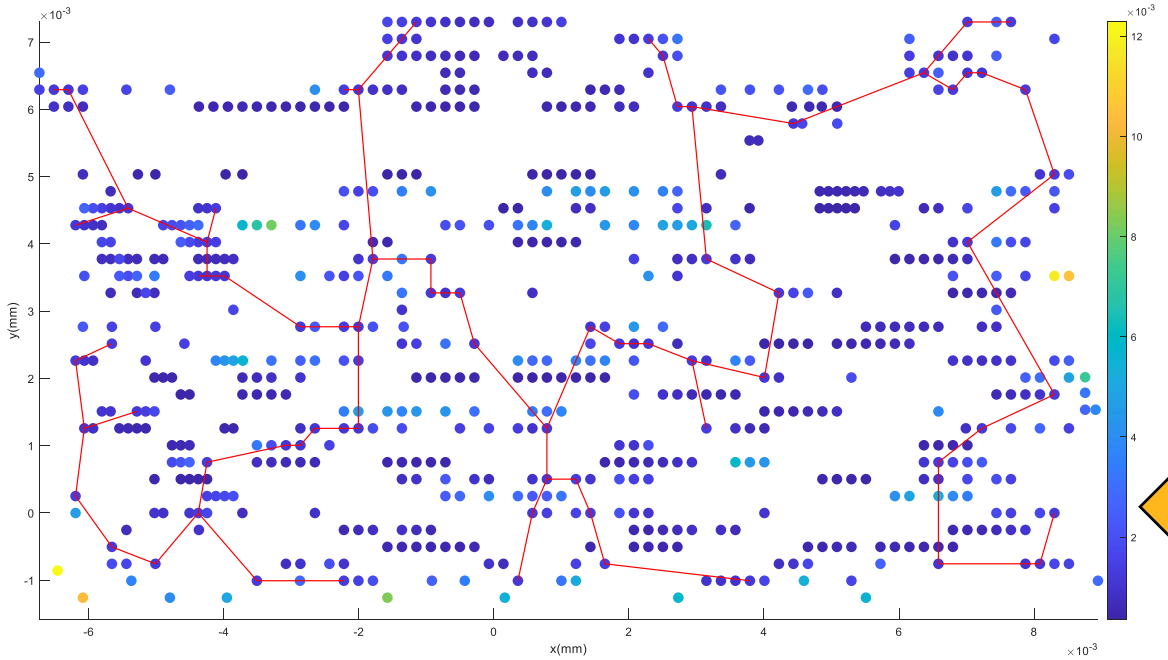
- Adaptive process update and messaging in real time for CPA-Q3D solver

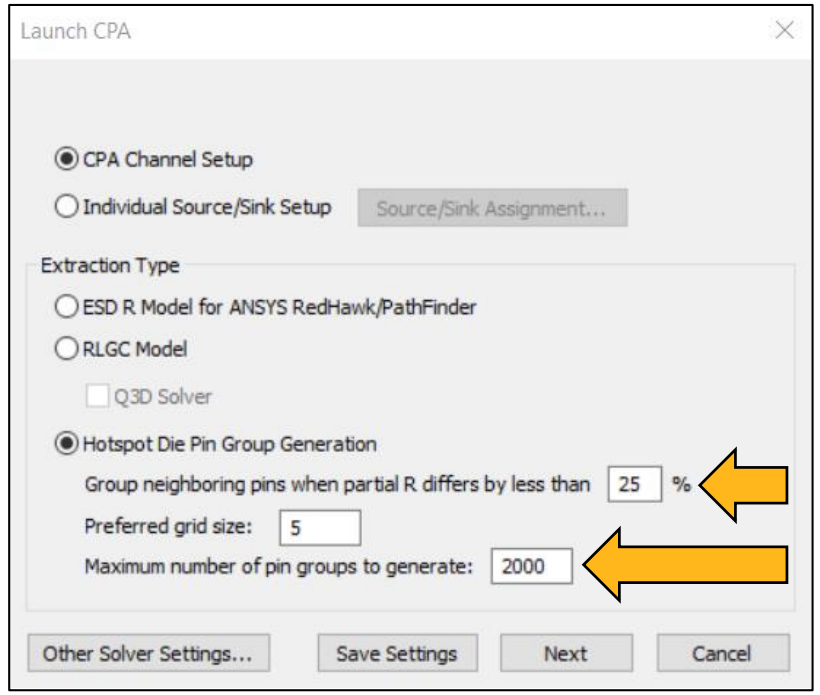




CPA Solver

- Smart pin group enhancements
  - Cluster-based pin grouping algorithm with user-specified percentage (ΔR) maximum pin group number





One connected pin group on colormap

- PLOC to smart pin group matching
  - Apply hotspot pin groups to die components by preserving the PLOC connectivity data

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